

### FEATURES

#### AC PERFORMANCE

Unity Gain Bandwidth: 34 MHz  
Fast Settling: 135 ns to 0.01%  
Slew Rate: 250 V/ $\mu$ s  
Stable at Gains of 1 or Greater  
Full Power Bandwidth: 3.9 MHz

#### DC PERFORMANCE

Input Offset Voltage: 1 mV max (AD843K/B)  
Input Bias Current: 0.6 nA typ  
Input Voltage Noise: 19 nV/ $\sqrt{\text{Hz}}$   
Open Loop Gain: 30 V/mV into a 500  $\Omega$  Load  
Output Current: 50 mA min  
Supply Current: 13 mA max

Available in 8-Pin Plastic Mini-DIP & Cerdip, 16-Pin SOIC, 20-Pin LCC and 12-Pin Hermetic Metal Can Packages  
Available in Tape and Reel in Accordance with EIA-481A Standard

Chips and MIL-STD-883B Parts Also Available

#### APPLICATIONS

High Speed Sample-and-Hold Amplifiers  
High Bandwidth Active Filters  
High Speed Integrators  
High Frequency Signal Conditioning

### PRODUCT DESCRIPTION

The AD843 is a fast settling, 34 MHz, CBFET input op amp. The AD843 combines the low (0.6 nA) input bias currents characteristic of a FET input amplifier while still providing a 34 MHz bandwidth and a 135 ns settling time (to within 0.01% of final value for a 10 volt step). The AD843 is a member of the Analog Devices' family of wide bandwidth operational amplifiers. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp.

The 250 V/ $\mu$ s slew rate and 0.6 nA input bias current of the AD843 ensure excellent performance in high speed sample-and-hold applications and in high speed integrators. This amplifier is also ideally suited for high bandwidth active filters and high frequency signal conditioning circuits.

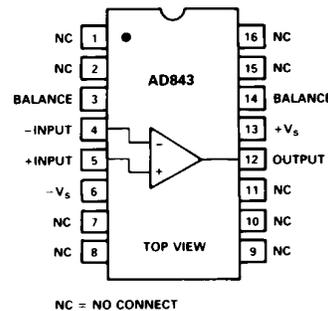
Unlike many high frequency amplifiers, the AD843 requires no external compensation and it remains stable over its full operating temperature range. It is available in five performance grades: the AD843J and AD843K are rated over the commercial temperature range of 0°C to +70°C. The AD843A and AD843B are rated over the industrial temperature range of -40°C to +85°C. The AD843S is rated over the military temperature range of -55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

### REV. D

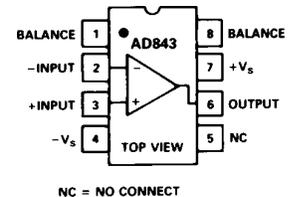
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### CONNECTION DIAGRAMS

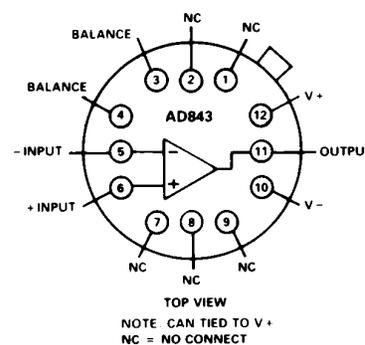
#### 16-Pin SOIC (R-16) Package



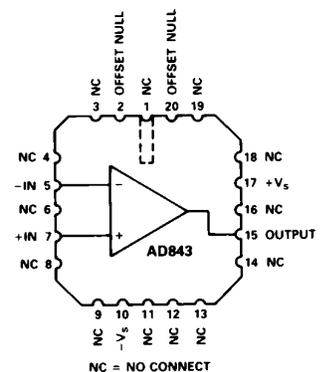
#### Plastic (N-8) and Cerdip (Q-8) Package



#### TO-8 (H-12A) Package



#### LCC (E-20A) Package



The AD843 is offered in either 8-pin plastic DIP or hermetic cerdip packages, in 16-pin SOIC, 20-Pin LCC, or in a 12-pin metal can. Chips are also available.

### PRODUCT HIGHLIGHTS

1. The high slew rate, fast settling time and low input bias current of the AD843 make it the ideal amplifier for 12-bit D/A and A/D buffers, for high speed sample-and-hold amplifiers and for high speed integrator circuits. The AD843 can replace many FET input hybrid amplifiers such as the LH0032, LH4104 and OPA600.
2. Fully differential inputs provide outstanding performance in all standard high frequency op amp applications such as signal conditioning and active filters.
3. Laser wafer trimming reduces the input offset voltage to 1 mV max (AD843K and AD843B).
4. Although external offset nulling is unnecessary in many applications, offset null pins are provided.
5. The AD843 does not require external compensation at closed loop gains of 1 or greater.

# AD843—SPECIFICATIONS (@ $T_A = +25^\circ\text{C}$ and $\pm 15\text{ V dc}$ , unless otherwise noted)

Model	Conditions	AD843J/A			AD843K/B			AD843S <sup>1</sup>			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE <sup>1</sup> Offset Drift	$T_{\text{MIN}}-T_{\text{MAX}}$	1.0	2.0		0.5	1.0		1.0	2.0		mV
		1.7	4.0		1.2	2.0		3.0	4.5		mV
INPUT BIAS CURRENT	Initial ( $T_J = +25^\circ\text{C}$ )	50			40			50			pA
	Warmed-Up <sup>2</sup> $T_{\text{MIN}}-T_{\text{MAX}}$	0.8	2.5	60/160	0.6	1.0	23/65	0.8	2.5	2600	nA nA
INPUT OFFSET CURRENT	Initial ( $T_J = +25^\circ\text{C}$ ) Warmed-Up <sup>2</sup> $T_{\text{MIN}}-T_{\text{MAX}}$	30			20			30			pA
		0.25	1.0	23/64	0.2	0.4	9/26	0.25	1.0	1025	nA nA
INPUT CHARACTERISTICS Input Resistance Input Capacitance		$10^{10}$			$10^{10}$			$10^{10}$			$\Omega$
		6			6			6			pF
INPUT VOLTAGE RANGE Common Mode		$\pm 10$	+12, -13		$\pm 10$	+12, -13		$\pm 10$	+12, -13		V
COMMON-MODE REJECTION	$V_{\text{CM}} = \pm 10\text{ V}$ $T_{\text{MIN}}-T_{\text{MAX}}$	60	72		70	76		60	72		dB
		60	72		68	76		60	72		dB
INPUT VOLTAGE NOISE Wideband Noise	$f = 10\text{ kHz}$ 10 Hz to 10 MHz	19			19			19			$\text{nV}/\sqrt{\text{Hz}}$ $\mu\text{V rms}$
OPEN LOOP GAIN	$V_O = \pm 10\text{ V}$ $R_{\text{LOAD}} \geq 500\ \Omega$ $T_{\text{MIN}}-T_{\text{MAX}}$	15	25		20	30		15	30		V/mV
		10	20		10	25		10	25		V/mV
OUTPUT CHARACTERISTICS Voltage Current Output Resistance	$R_{\text{LOAD}} \geq 500\ \Omega$ $V_{\text{OUT}} = \pm 10\text{ V}$ Open Loop	$\pm 10$	+11.5, -12.6		$\pm 10$	+11.5, -12.6		$\pm 10$	+11.5, -12.6		V
		50	12		50	12		50	12		mA $\Omega$
FREQUENCY RESPONSE Unity Gain Bandwidth Full Power Bandwidth <sup>3</sup>	$V_{\text{OUT}} = 90\text{ mV p-p}$ $V_O = 20\text{ V p-p}$ $R_I \geq 500\ \Omega$	34			34			34			MHz
		2.5	3.9		2.5	3.9		2.5	3.9		MHz
Rise Time	$A_{\text{VCL}} = -1$		10			10			10		ns
Overshoot	$A_{\text{VCL}} = -1$		15			15			15		%
Slew Rate	$A_{\text{VCL}} = -1$	160	250		160	250		160	250		V/ $\mu\text{s}$
Settling Time	$A_{\text{VCL}} = -1$ to 0.1% to 0.01%		95			95			95		ns
			135			135			135		ns
Overdrive Recovery	-Overdrive +Overdrive		200			200			200		ns
			700			700			700		ns
Differential Gain	$f = 4.4\text{ MHz}$		0.025			0.025			0.025		%
Differential Phase	$f = 4.4\text{ MHz}$		0.025			0.025			0.025		Degree
POWER SUPPLY Rated Performance Operating Range Quiescent Current	$T_{\text{MIN}}-T_{\text{MAX}}$ $\pm 5\text{ V to } \pm 18\text{ V}$ $T_{\text{MIN}}-T_{\text{MAX}}$	$\pm 4.5$	$\pm 15$	$\pm 18$	$\pm 4.5$	$\pm 15$	$\pm 18$	$\pm 4.5$	$\pm 15$	$\pm 18$	V V mA
			12	13		12	13		12	13	
Rejection Ratio Rejection Ratio	$T_{\text{MIN}}-T_{\text{MAX}}$ $\pm 5\text{ V to } \pm 18\text{ V}$ $T_{\text{MIN}}-T_{\text{MAX}}$	65	76	14	70	80	14	65	76	16	dB dB
		62	76		68	80		62	76		
TEMPERATURE RANGE Operating, Rated Performance Commercial ( $0^\circ\text{C to } +70^\circ\text{C}$ ) Industrial ( $-40^\circ\text{C to } +85^\circ\text{C}$ ) Military ( $-55^\circ\text{C to } +125^\circ\text{C}$ ) <sup>4</sup>		AD843J AD843A			AD843K AD843B			AD843S			
PACKAGE OPTIONS Plastic (N-8) Cerdip (Q-8) Metal Can (H-12A) LCC (E-20A) SOIC (R-16) Tape & Reel Chips		AD843JN AD843AQ  AD843JR-16 AD843JR-16-REEL AD843JR-16-REEL7 AD843JCHIPS			AD843KN AD843BQ AD843BH			AD843SQ, AD843SQ/883B AD843SH, AD843SH/883B AD843SE/883B  AD843SCHIPS			

NOTES

<sup>1</sup>Standard Military Drawings Available: 5962-9098001M2A (SE/883B), 5962-9098001MXA (SH/883B), 5962-9098001MPA (SQ/883B).

<sup>2</sup>Specifications are guaranteed after 5 minutes at  $T_A = +25^\circ\text{C}$ .

<sup>3</sup>Full power bandwidth = Slow Rate/2  $\pi\text{V}$  peak.

<sup>4</sup>All "S" grade  $T_{\text{MIN}}-T_{\text{MAX}}$  specifications are tested with automatic test equipment at  $T_A = -55^\circ\text{C}$  and  $T_A = +125^\circ\text{C}$ .

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed although only those shown in **boldface** are tested on all production units.

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

Supply Voltage	$\pm 18\text{ V}$
Internal Power Dissipation <sup>2</sup>	
Plastic Package	1.50 Watts
Cerdip Package	1.35 Watts
12-Pin Header Package	1.80 Watts
16-Pin SOIC Package	1.50 Watts
20-Pin LCC Package	1.00 Watt
Input Voltage	$\pm V_S$
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range (N, R)	$-65^\circ\text{C}$ to $+125^\circ\text{C}$
Storage Temperature Range (Q, H, E)	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Operating Temperature Range	
AD843J/R	$0^\circ\text{C}$ to $+70^\circ\text{C}$
AD843A/B	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
AD843S	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60 sec)	$+300^\circ\text{C}$
ESD Rating	500 V

NOTES

<sup>1</sup>Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

<sup>2</sup>8-Pin Plastic Package:  $\theta_{JA} = 100^\circ\text{C/Watt}$

8-Pin Cerdip Package:  $\theta_{JA} = 110^\circ\text{C/Watt}$

12-Pin Header Package:  $\theta_{JA} = 80^\circ\text{C/Watt}$

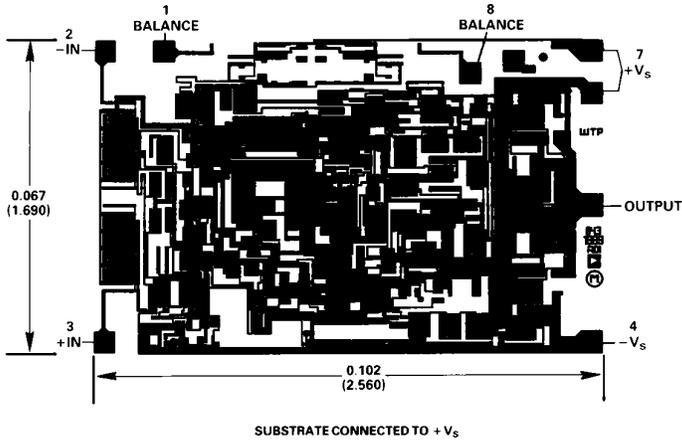
16-Pin SOIC Package:  $\theta_{JA} = 100^\circ\text{C/Watt}$

20-Pin LCC Package:  $\theta_{JA} = 150^\circ\text{C/Watt}$

**METALIZATION PHOTOGRAPH**

Contact factory for latest dimensions.

Dimensions shown in inches and (mm).



# AD843—Typical Characteristics

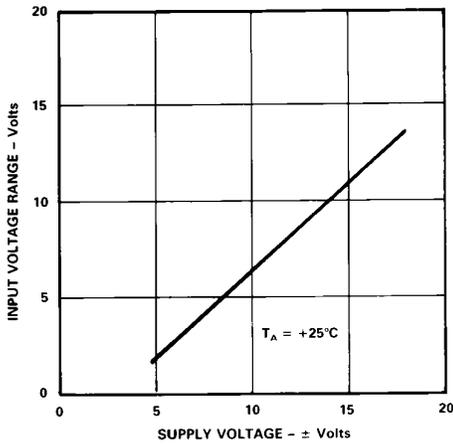


Figure 1. Input Voltage Range vs. Supply Voltage

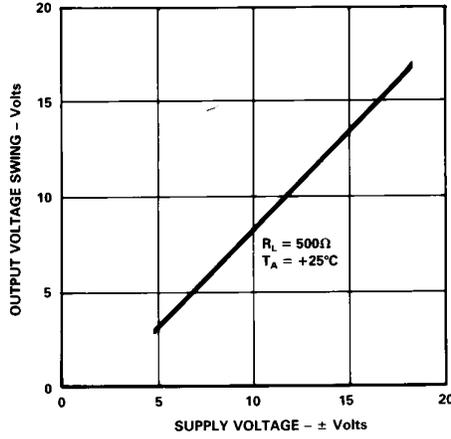


Figure 2. Output Voltage Swing vs. Supply Voltage

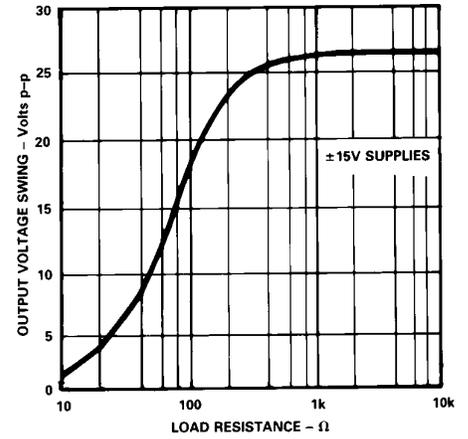


Figure 3. Output Voltage Swing vs. Load Resistance

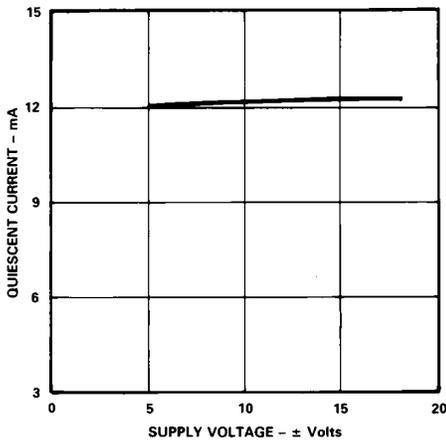


Figure 4. Quiescent Current vs. Supply Voltage

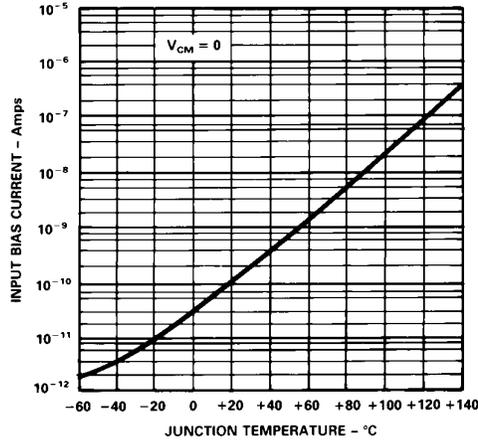


Figure 5. Input Bias Current vs. Junction Temperature

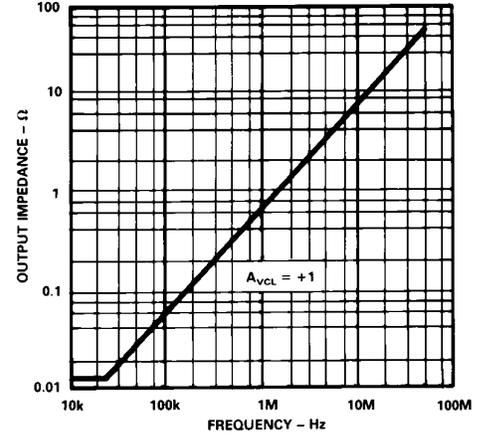


Figure 6. Output Impedance vs. Frequency

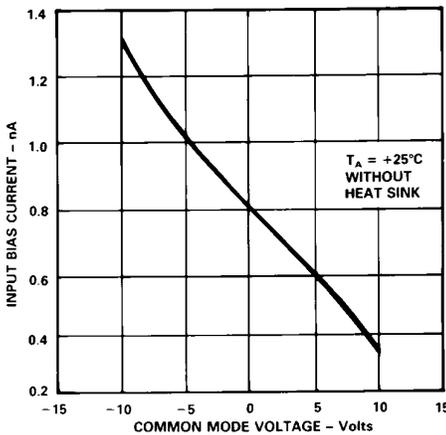


Figure 7. Input Bias Current vs. Common Mode Voltage

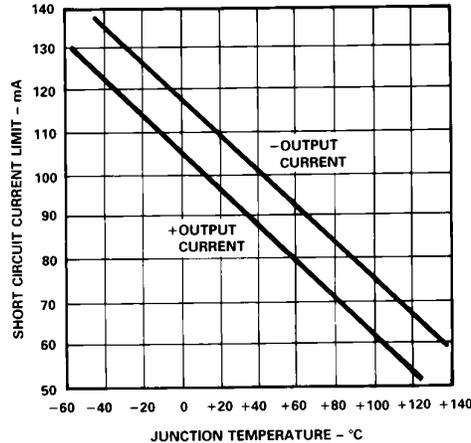


Figure 8. Short Circuit Current Limit vs. Junction Temperature ( $T_J$ )

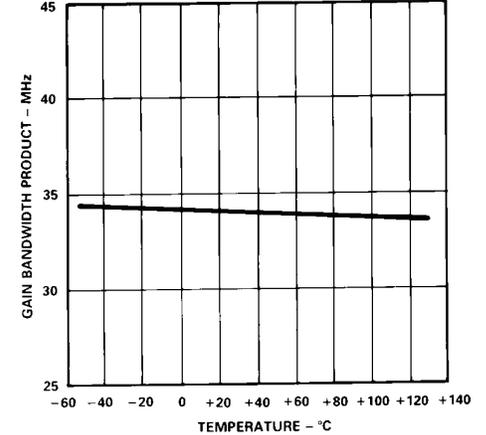


Figure 9. Gain Bandwidth Product vs. Temperature

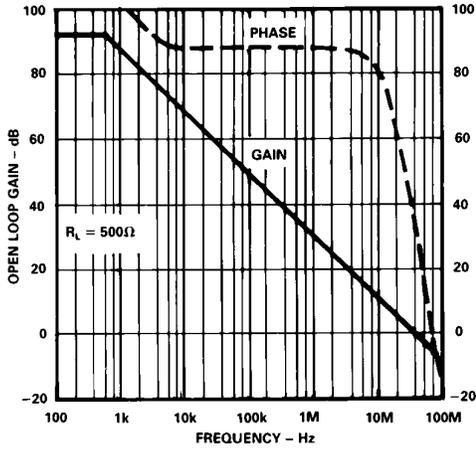


Figure 10. Open Loop Gain and Phase Margin vs. Frequency

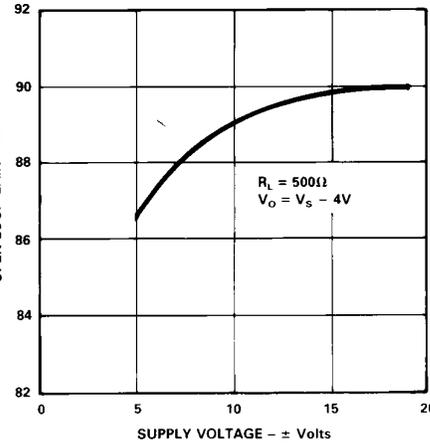


Figure 11. Open Loop Gain vs. Supply Voltage

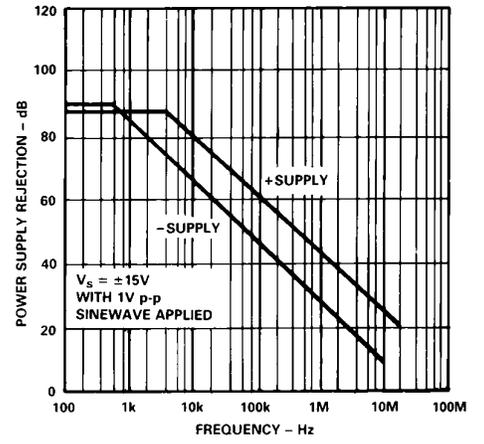


Figure 12. Power Supply Rejection vs. Frequency

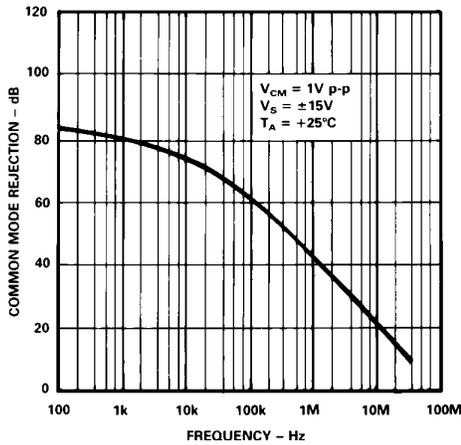


Figure 13. Common Mode Rejection vs. Frequency

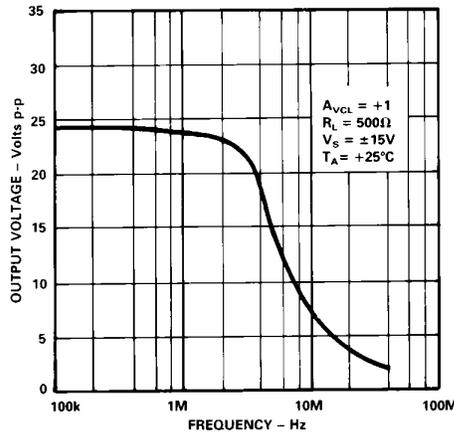


Figure 14. Large Signal Frequency Response

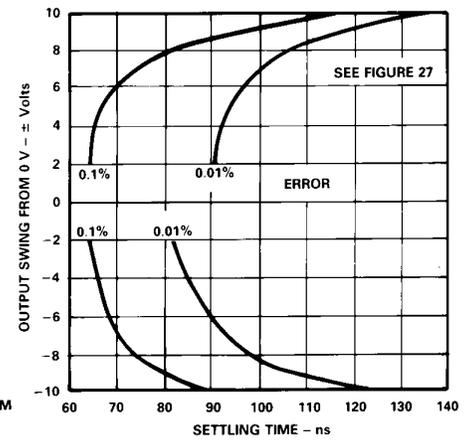


Figure 15. Output Swing and Error vs. Settling Time

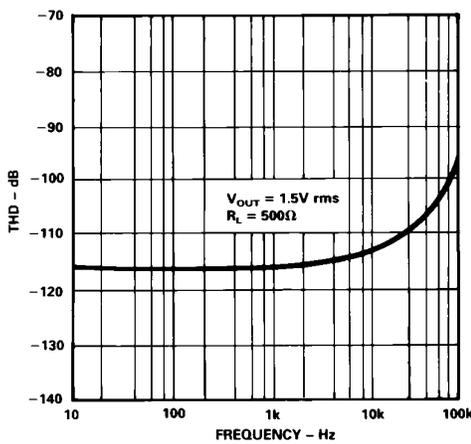


Figure 16. Harmonic Distortion vs. Frequency

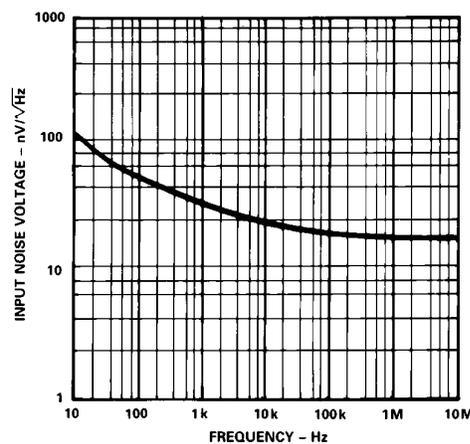


Figure 17. Input Noise Voltage Spectral Density

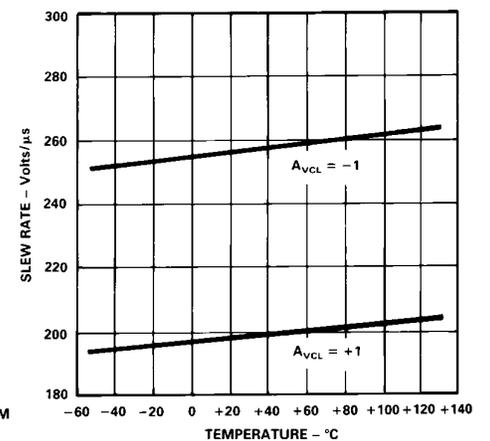


Figure 18. Slew Rate vs. Temperature

# AD843—Typical Characteristics

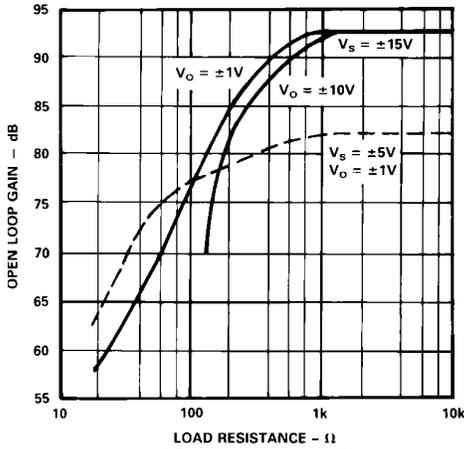


Figure 19. Open Loop Gain vs. Resistive Load

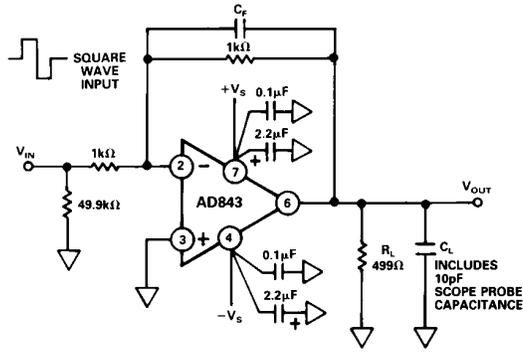


Figure 20a. Inverting Amplifier Connection

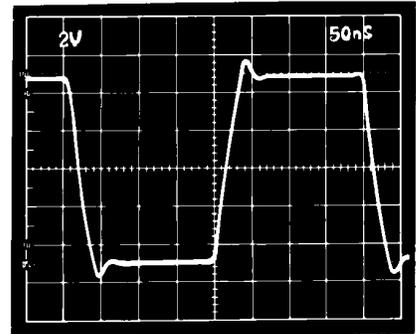


Figure 20b. Inverter Large Signal Pulse Response.  $C_f = 0$ ,  $C_L = 10$  pF

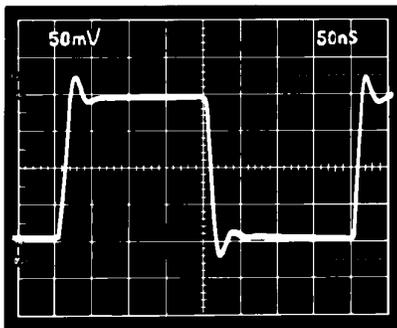


Figure 20c. Inverter Small Signal Pulse Response.  $C_f = 0$ ,  $C_L = 10$  pF

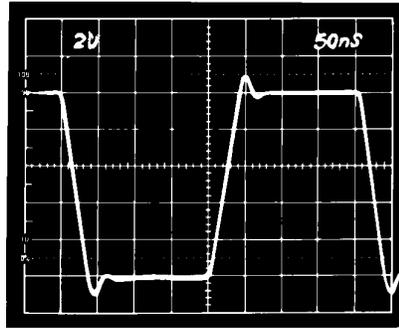


Figure 20d. Inverter Large Signal Pulse Response.  $C_f = 5$  pF,  $C_L = 110$  pF

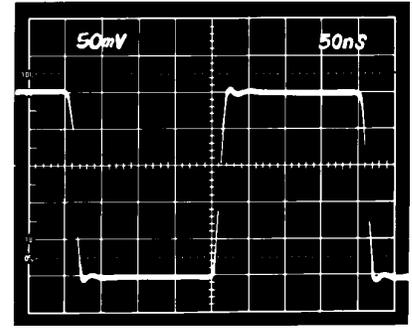


Figure 20e. Inverter Small Signal Pulse Response.  $C_f = 5$  pF,  $C_L = 110$  pF

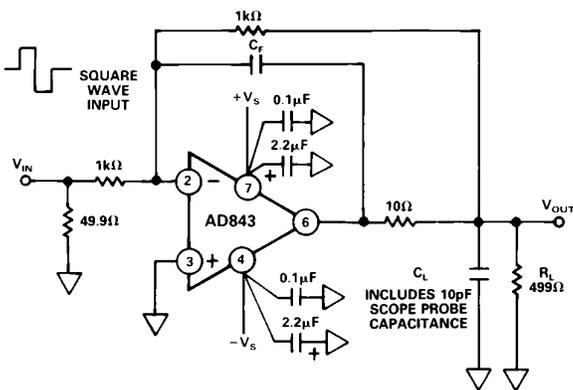


Figure 21a. Unity Gain Inverter Circuit for Driving Capacitive Loads

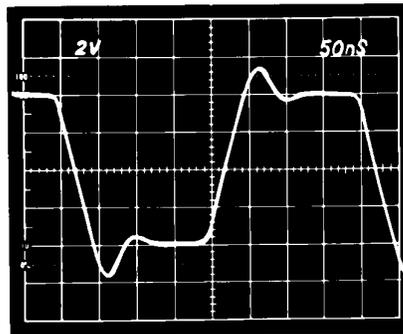


Figure 21b. Inverter Cap Load Large Signal Pulse Response.  $C_f = 15$  pF,  $C_L = 410$  pF

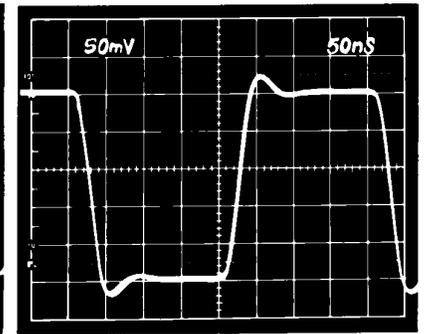


Figure 21c. Inverter Cap Load Small Signal Pulse Response.  $C_f = 15$  pF,  $C_L = 410$  pF

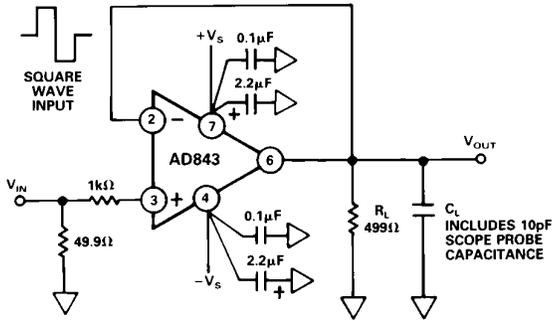


Figure 22a. Unity Gain Buffer Amplifier

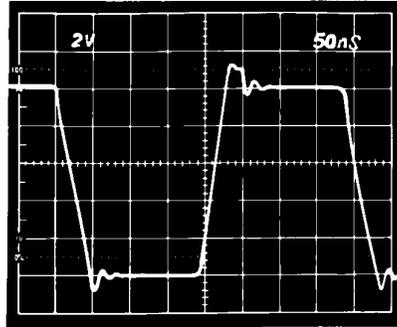


Figure 22b. Buffer Large Signal Pulse Response.  $C_L = 10 \text{ pF}$

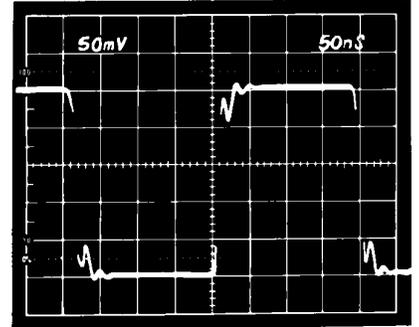


Figure 22c. Buffer Small Signal Pulse Response.  $C_L = 10 \text{ pF}$

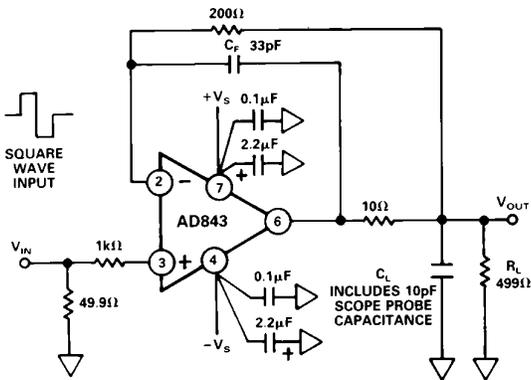


Figure 23a. Unity Gain Buffer Circuit for Driving Capacitive Loads

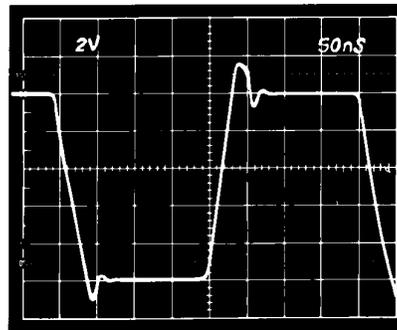


Figure 23b. Buffer Cap Load Large Signal Pulse Response.  $C_F = 33 \text{ pF}$ ,  $C_L = 10 \text{ pF}$

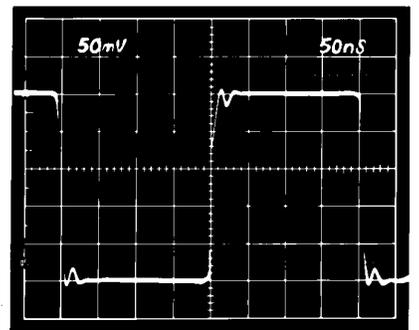


Figure 23c. Buffer Cap Load Small Signal Pulse Response.  $C_F = 33 \text{ pF}$ ,  $C_L = 10 \text{ pF}$

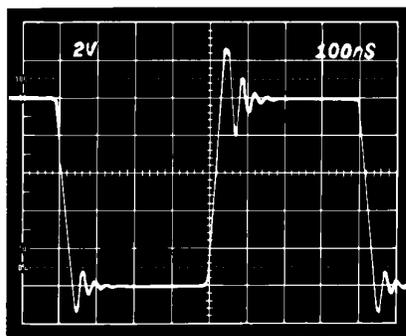


Figure 23d. Buffer Cap Load Large Signal Pulse Response.  $C_F = 33 \text{ pF}$ ,  $C_L = 110 \text{ pF}$

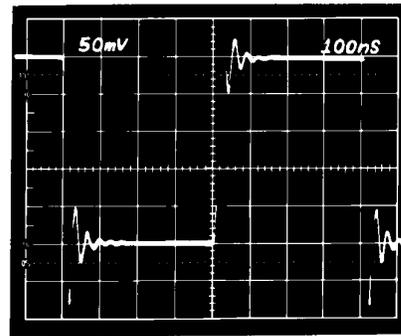


Figure 23e. Buffer Cap Load Small Signal Pulse Response.  $C_F = 33 \text{ pF}$ ,  $C_L = 110 \text{ pF}$